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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,495	02/11/2002	William A. Stevens, JR.	042390.P9143	6012

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/073,495	STEVENS, ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 26, 2007 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "invoking a function contained in a third firmware module during a dispatch of the earlier firmware module or the later firmware module, wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 42 is objected to because of the following informalities: "after initializing a plurality of firmware modules" should be "after initializing the plurality of firmware modules". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 48 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant did not disclose "invoking a function contained in a third firmware module during a dispatch of the earlier firmware module or the later firmware module, wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked" in the original specification. Examiner was not able to find any disclosure on invoking a function contained in a third firmware module during a dispatch of one of the two initial firmware

modules, when the third firmware module is dispatched subsequent to the two initial firmware modules. Examiner will take the position that the function is invoked after the third firmware module is dispatched [i.e., after the two initial firmware modules] in order to apply prior art.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 42, 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Stevens, US Patent 6633976.

8. In re claim 42, Stevens discloses a method comprising:

- Initializing a plurality of firmware modules [col.2, l.48 – col.3, l.15], wherein the initializing comprises:
    - Examining at least two firmware modules [module to initialize CPU, module to initialize memory] to determine a required order of dispatch of the firmware modules [col.2, ll.59-60; col.3, ll.2-3; examination of modules and determination of required order of dispatch may be coded before runtime].
    - Dispatching an earlier of the two firmware modules and then dispatching a later of the two firmware modules [ordered execution of initialization modules results in one module being the earlier and the other being the later] [col.3, ll.2-3].

- After initializing the plurality of firmware modules, initializing a system memory [system memory is initialized after initialization modules are dispatched [col.3, ll.2-3].

9. As to claim 48, Stevens taught each and every limitation of the claim as discussed above. Stevens discloses invoking a function [e.g., sequential execution] contained in a third firmware module [e.g., dispatch manager], wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked [firmware module is dispatched first before function in firmware module can be executed] [col.3, ll.1-6; function invoked after third firmware module is dispatched after the ordered dispatching of the first two firmware modules].

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 43-44, 50-51, 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens as applied to claim 42 above, and further in view of Patel, US Patent 5999989.

12. Stevens discloses each and every limitation of the claim as discussed above. Stevens discloses executing a core module [dispatch manager] by determining a requirements configuration of the plurality of firmware modules [additional modules] appropriate to run [col.2, l.60; col.3, ll.17-31].

13. Stevens did not discuss details involving a resource list; examining a platform to determine whether hardware to be initialized by the module is present in the platform.

14. In re claim 43, Patel discloses, wherein examining comprises checking a resource list of each of the two firmware modules [associated with BIOS] [col.12, ll.7-18].

15. In re claim 44, Patel discloses, wherein the initialization [POST part of initialization] of the plurality of firmware modules comprises examining a platform to determine whether hardware to be initialized by the module is present in the platform [col.14, ll.13-26].

16. In re claim 50, Stevens discloses a computer-readable medium containing instructions [initialization code] to cause a programmable processor [that runs initialization code] to perform operations comprising initializing a volatile memory [RAM] after dispatching the plurality of firmware modules [module to initialize CPU, module to initialize memory] [col.3, ll.2-3; col.5, ll. 37-39].

17. Stevens did not discuss the details of determining dependencies among a plurality of firmware modules based on information about services imported and exported by each of the firmware modules

18. Patel discloses a computer-readable medium [system ROM] containing instructions to cause a programmable processor [e.g., CPU] to perform operations [col.2, ll.39-49; col.3, ll.40-43] comprising determining dependencies among a plurality of firmware modules [option ROMs associated with devices] based on information about services imported [part of ROM header data structure] and exported [via register arguments] by each of the firmware modules [col.1, ll.51-56; col.7, ll.1-42; col.8, ll.6-46]. Patel did not disclose explicitly dispatching each module of the plurality of firmware modules in an order that satisfies the dependencies. Examiner had taken Official Notice that it is well known in the art to dispatch modules in an order based on

dependencies, as the meaning of dependencies inherently involves an ordering [e.g., parent must come before child].

19. As to claim 51, Patel discloses, wherein the information about services imported and exported by a firmware comprises an export table [interrupt table] containing at least one service provided by the firmware module [col.7, ll.1-29; col.8, ll.6-46; interrupts associated with calls].

20. As to claim 53, Patel discloses, wherein dispatching a module comprises saving a return address in a processor register [far return to POST; address saved in processor register as is well known in the art] and executing a beginning instruction of the module [e.g., performs device specific write-protection] [col.7, ll.1-29, ll.43-47].

21. In re claim 54, Stevens discloses a system [fig.2] comprising:

- A hardware component [e.g., 11] to perform a function [e.g., execute instructions].
- A volatile memory [13] that can store data after the volatile memory is initialized.
- A non-volatile memory [15, 20a] containing a BIOS including a BIOS core and a plurality of firmware modules [16, 17, n modules in 20a].
- Wherein two of the plurality of firmware modules [e.g., module to initialize CPU, module to initialize system memory] are to initialize hardware components [e.g., cpu, system memory] to perform the function [col.2, ll.4-11; col.3, ll.1-3].
- Said two of the plurality of firmware modules are to be dispatched before the volatile memory is initialized [col.3, ll.1-3].

22. Stevens did not disclose the situation where a hardware component is not present in the system.

23. Patel discloses a system [analogous to Stevens] wherein one of the two firmware modules is to initialize a hardware component [devices] that is not present in the system [fig.2; col.6, ll.10-47; if one of the hardware component is not present, steps 206-218 are repeated with one of the firmware module taken out of dispatched allocation map].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Patel before him at the time the invention was made, to modify the system taught by Stevens to include the teachings of Patel, in order to obtain the claimed method and system, including wherein the initializing of the plurality of firmware modules further comprises executing a core module by determining a requirements configuration of the plurality of firmware modules appropriate to run [col.3, ll.40-48; run Stevens core module statically instead of via system memory to conserve memory resource]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of BIOS operation [Patel: col.1, ll.51-56; e.g., Patel's teaching enhances Stevens' early initialization by enabling the determination of whether the system memory or required resources is present or not] while conserving memory resource.

25. As to claim 55, Stevens discloses, wherein the volatile memory is a RAM [col.4, l.37].

26. As to claim 56, Stevens discloses, wherein the non-volatile memory is at least one of a ROM or a flash memory [col.5, ll.1-26].

27. Claims 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens as applied to claim 42 above, and further in view of Ayers et al., US Patent 6353924, hereinafter Ayers.

28. Stevens taught each and every limitation of the claim as discussed above. Stevens did not disclose explicitly marking a data structure after dispatching a firmware module.

29. In re claim 45, Ayers discloses a method comprising marking a data structure [e.g., table] after dispatching a firmware module [e.g., block], wherein the data structure is to indicate whether the firmware module has been dispatched [col.4, ll.51-58].

30. As to claim 46, Ayers discloses, wherein the data structure is a bit array [circular buffer] [col.4, ll.17-19].

31. As to claim 47, Ayers discloses, wherein the data structure is held in a processor register [col.4, ll.5-16].

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Ayers before him at the time the invention was made, to modify the system taught by Stevens to include the explicit well known data structure teachings of Ayers, as using data structures to record an event [e.g., dispatched firmware module] is very well known and suitable for use in the system of Stevens. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to record events and aid debugging efforts [Ayers: col.1, ll.1-30].

33. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens as applied to claim 48 above, and further in view of Patel and Katayama et al., US Publication 20010007119, hereinafter Katayama.

34. Stevens taught each and every limitation of the claim as discussed above. Stevens did not disclose explicitly scanning to find a module that operates with a hardware component present in

the platform and invoking the function if such a module is found and did not disclose explicitly the firmware modules being arranged in a daisy chain.

35. Patel discloses scanning to find a module that operates with a hardware component present in the platform and invoking the function if such a module is found [col.6, ll.10-48].

36. Katayama discloses a method comprises a daisy chain of [firmware] modules [e.g., 85, 91] [0107-0109].

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Patel, Stevens and Katayama before him at the time the invention was made, to modify the system taught by Stevens to include the teachings of Patel and the explicit well known daisy chain teachings of Katayama, as using daisy chains to organize related objects [e.g., firmware module] is very well known and suitable for use in the system of Stevens. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of BIOS operation [Patel: col.1, ll.51-56; e.g., Patel's teaching enhances Stevens' early initialization by enabling the determination of whether the system memory or required resources is present or not] and organize data that allows continuous access without the data being required to be stored in a continuous location [Katayama: 0109].

38. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Patel as applied to claim 50 above, and further in view of Ayers as applied to claim 45 and 47 above.

Response to Arguments

39. Applicant's arguments filed March 26, 2007 have been fully considered but they are not persuasive.

40. As discussed above, the drawings remain rejected for not showing the feature "invoking a function contained in a third firmware module during a dispatch of the earlier firmware module or the later firmware module, wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked". Applicant argues that this feature is shown in figure 10, where "a 'daisy chaining operation' is invoked in firmware module 212C during the execution/dispatch of firmware modules 212A or 212B". Examiner disagrees and submits that the daisy chaining operation is not a function to be invoked in firmware module 212C, but is a general description of how the firmware modules are linked [i.e., overall operation flows from one firmware module to the next in a daisy chained fashion]. In effect, figure 10 shows a function [1003C] being invoked after the third firmware module [212C] is dispatched after the two initial firmware modules [212A and 212B].

41. Similarly, claim 48 remains rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicant's specific citations in reference to the "daisy chaining operation" does not teach show the claimed method invoking a function contained in a third firmware module during a dispatch of one of the two initial firmware modules, when the third firmware module is dispatched subsequent to the two initial firmware modules.

42. Applicant argues that Stevens did not disclose "after initializing a plurality of firmware modules, initializing a system memory". Examiner disagrees and submits that the module to initialize CPU and the module to initialize memory are considered to be a plurality of firmware modules that are initialized before the system memory [i.e., the initialization code modules that are to be executed prior to other modules]. This is in accordance with Applicant's own teaching

of having one of modules 212-1 to 212-M initialize memory before initializing other modules [e.g., add-ons] [Applicant's Specification: pg. 8, ll.2-9].

43. Applicant's arguments with respect to claim 50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
April 28, 2007